Photoactive Memory by a Si-Nanowire Field-Effect Transistor

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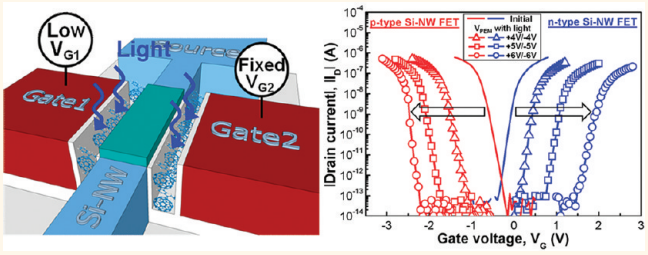
ABSTRACT



A photoactive memory is implemented on a n-type and p-type double-gate silicon nanowire (Si-NW) field-effect transistor (FET) through the grafting of solution-processable [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM) in nanogaps. Despite integration with organic material, superior FET characteristics are observed. Lowered operation voltage is achieved through the use of an optical source and an efficient photon-absorbing structure. Due to the naturally separated gate structure for PCBM embedment, moreover, memory performances stemming from a photoactive property are notably improved by biasing asymmetric voltage to the separated gates, which are individually controlled. The development of photoactive Si-NW FET based on CMOS process can pave the way of optoelectronic applications with more degree of freedom in terms of overall device design.

KEYWORDS: silicon nanowire · field-effect transistor · nanogap · double-gate · memory · photoelectrical program · PCBM · threshold voltage

Nanogaps, which are formed through the release of a sacrificial layer, have garnered interest in a number of regards from the research community. First, researchers have started to take note of the nanogaps' capability to define a sublithographically scaled space easily and cost effectively. Nanogaps fabricated by various methods are used for the purposes of electrode formation and surface-enhanced raman spectroscopy (SERS).[1,2] Second, an empty nanogap can serve as a nanofluidic channel, allowing the flow of solutions containing target materials such as molecules and DNA. Through the electrostatic changes in the nanogap, a nanogap-embedded device can detect the target materials without a labeling procedure.[3−5] Third, the nanogap offers multifaceted applications with numerous materials through combinatorial integrations. Materials vulnerable to high temperature, such as organic and high-*k* materials, can be grafted in the prepared nanogap after all high-temperature processes are completed. These nanogap-based structures facilitate the use of organic or high-*k* materials for nonvolatile memory applications (Figure 1a).[6−8]

To make the best use of a nanogap structure in device applications, the choice of target material to graft is an important issue. It was demonstrated that a FET grafted with photoactive organic material can be operated for memory application (Figure 1b).[9] In particular, it dramatically reduced program/erase operation voltages compared with the use of only an electrical program method. However, structure characterized by the incorporation of lateral nanogaps in a planar structured device has a key disadvantage owing to the position of the poly-Si electrode located on top of the photon-absorbing material, which serves as a source of memory operation, hindering absorption of incident light.[10] In addition, a small fraction of the photon-absorbing material partially occupying a channel may sacrifice the efficiency of the memory characteristics. The planar device structure based on a single gate showed n-channel characteristics only; moreover, it cannot overcome the impending limitation of device scaling.[11]

Herein, in an effort to overcome the aforementioned problems, we implement a memory device with photoactive characteristics on a n-type and p-type silicon-nanowire (Si-NW) FET composed of separated double gates (DG) and completely opened nanogaps, which can harness a Si-NW channel entirely wrapped by the photoactive material. Furthermore, the proposed device maintains the strengths of silicon devices such as high-quality FET properties and reliable characteristics. It should be

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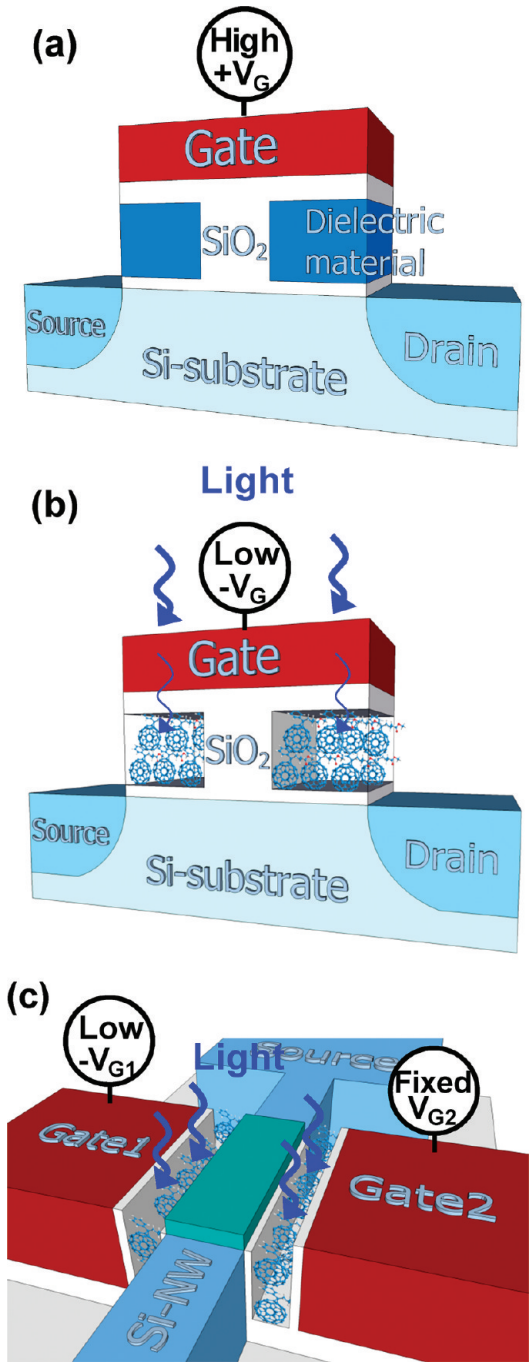

Figure 1. Evolution of a nanogap-embedded device for memory applications. Schematic of the lateral nanogap-embedded single-gate FET operating with (a) an electrical program method and (b) a photoelectrical- program method with light. The photoelectrical program lowers the operation voltage compared to the electrical program alone. (c) Schematic of the vertical nanogap-embedded double-gate Si-NW FET operating with a photoelectrical program method with light. The photoactive PCBM is embedded through the separated gates, and this structure makes possible independently controllable gates (Gate 1, Gate 2).

noted that a complementary (n-type and p-type) property is considered to be a key element to advance current microelectronics. It is thus important, and timely, to integrate photoactive memory to

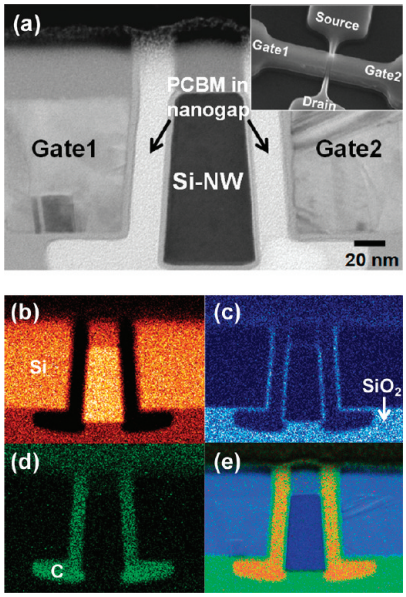

Figure 2. (a) Cross-sectional TEM image of the fabricated photoactive Si-NW. Inset shows a bird's eye view SEM image. EDS element mapping of (b) silicon (c) oxygen and (d) carbon. Panel e shows a mixed image of all elements.

demonstrate this type of complementary characteristic. To transform a Si-based NW FET operated electrically into a hybrid FET operated electrically and optically, photoactive and solution-processable C_{60}-derivative, [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM),[12,13] is embedded in nanogaps, which are located between both gates and the Si-NW channel. The proposed device with vertical nanogaps offers the advantage that polycrystalline Si (poly-Si) gate electrodes vertically standing at the sidewalls do not obstruct photon absorption of the PCBM material. Furthermore, by virtue of the separated gate structure as shown in Figure 1c, memory performance can be improved according to asymmetric gate bias, which allows further reduction of the operation voltage. The process flow of the independent double-gate Si-NW FET is described in the Methods section.

RESULTS AND DISCUSSION

Figure 2a shows a cross-sectional transmission electron microscopy (TEM) image of a fabricated Si-NW FET with a 50 nm wire width and 110 nm wire height. As can be inferred from Figure 2a, the n^+ (heavily doped) poly-Si gate to envelope the Si-NW is separated into two electrodes (Gate 1, Gate 2) by a chemical mechanical polishing (CMP) process, which uncovers the gate on the Si-NW selectively and exposes the sacrificial oxide to air. Thereafter, the previously deposited sacrificial oxide is removed by a wet etchant, thereby creating nanogaps. Thermal reoxidation is subsequently carried out to pzroduce the actual gate oxide. Afterward, the opened nanogaps are completely filled with dispersed PCBM molecules. The inset of Figure 2a

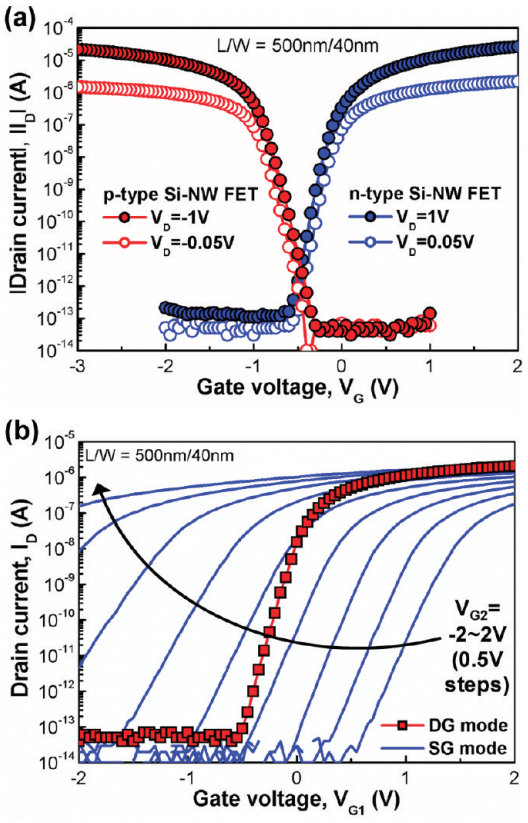

Figure 3. (a) I_D-V_G characteristics of the fabricated n-type and p-type Si-NW FETs with a gate length (L) of 500 nm and a wire width (W) of 40 nm. (b) I_D-V_G characteristics of the fabricated n-type Si-NW FET according to the SG mode and DG mode. In the SG mode, Gate 2 voltage is varied from −2 to 2 V with a step of 0.5 V.

shows a bird's eye view scanning electron microscopy (SEM) image of the NW FET with the vertical nanogaps before gap-filling.

Figure 2 panels b−e show cross-sectional energy dispersive X-ray spectroscopy (EDS) element mapping results of the fabricated Si-NW FET device. The oxygen mapping of Figure 2c clearly shows that the gate oxide is well grown for the isolation of PCBM from the Si-NW and poly-Si gates (compare the Si map of Figure 2b). These oxides at the Si-NW and gate side serve as an insulator for charge preservation generated by the following photoactive action. One oxide at the Si-NW side is named a tunneling oxide and the other oxide at the gate side is called a control oxide. It is noteworthy that the control oxide is thicker than the tunneling oxide due to different oxidation rates, which depend on dopant concentration.[14] This feature is very attractive for improvement of the nonvolatile memory characteristics. It should also be noted that the EDS element mapping of carbon in Figure 2d verifies complete gap filling of the nanogaps by the PCBM molecules, which were dominantly composed of carbon.

Figure 3a shows electrical characteristics of a PCBM-embedded n-type and a p-type Si-NW FET, respectively. Despite integration with organic material,

TABLE 1. The Electrical Performance of the Fabricated Photoactive n-Type and p-Type Si-NW FETs[a]

	subthreshold slope [mV/decade]	drain-induced barrier lowering [mV/V]
n-type Si-NW	70.3	79.8
p-type Si-NW	78.5	91.5

[a] Subthreshold slope (S.S.) value, which is a criterion for gate controllability over drain current, is defined as $dV_g/d \log I_d$ at the subthreshold region. The drain-induced barrier lowering (DIBL) value, as a criterion for V_T change immunity against short channel effect, is defined as $[V_T(@V_d = 1\ V) - (V_T(@V_d = 0.05\ V)]/[\text{high } V_d\ (1V) - \text{low } V_d\ \ (0.05\ V)]$.

outstanding drain current characteristics according to gate voltage (I_D-V_G, refer to Table 1) are obtained due to the nanogap structure, which allows PCBM insertion after all the CMOS processes with high temperature. Because the dielectric constant of PCBM is similar to that of the oxide,[15] the threshold voltage (V_T) of the n-channel, which is defined at V_G where I_D reaches 10 nA, is close to zero in a moderately doped channel.

Figure 3b compares I_D-V_G characteristics according to gate bias modes: single- and double-gate modes. Because of the separated gate structure, each gate can individually control the channel potential at each sidewall of the Si-NW.[16] A DG mode means that both gates are tied and they effectively control the channel potential more electrostatically compared to the following single-gate (SG) mode. Hence it shows improved I_D-V_G characteristics against short-channel effects. Figure S3 in the Supporting Information shows a V_T change and subthreshold slope according to a gate length for a DG mode and a single-gate (SG) mode, which represents a planar device with a single gate. When a gate length of a device shrinks, V_T roll-off and slope degradation are unavoidable due to the loss of gate controllability on the channel. These parameters indicate the better scalability of a DG device than that of a SG device. A SG mode means that Gate 1 is used as a drive gate for gate voltage sweep and Gate 2 is used as a supporting gate to provide fixed gate voltage, respectively. When Gate 2 bias is fixed at negative voltage, the value of which is smaller than the V_T extracted in the DG mode, the sidewall channel of NW near Gate 2 is depleted, and thus exhibits relatively lowered subthreshold slope (S.S.) but shows larger S.S. than with the DG mode. On the other hand, when Gate 2 bias is fixed at positive voltage, the value of which is greater than the V_T extracted in the DG mode, the sidewall channel of NW near Gate 2 is inverted. Accordingly, V_T and S.S. values are worsened rapidly compared to those under negative Gate 2 bias.

Figure 4 displays the unique photoactive characteristic at the DG mode by combination of electrical and optical pulses. As shown in Figure S2 of the Supporting Information, the initial I_D-V_G curve is barely affected by white light alone. However, the Si-NW FET shows a

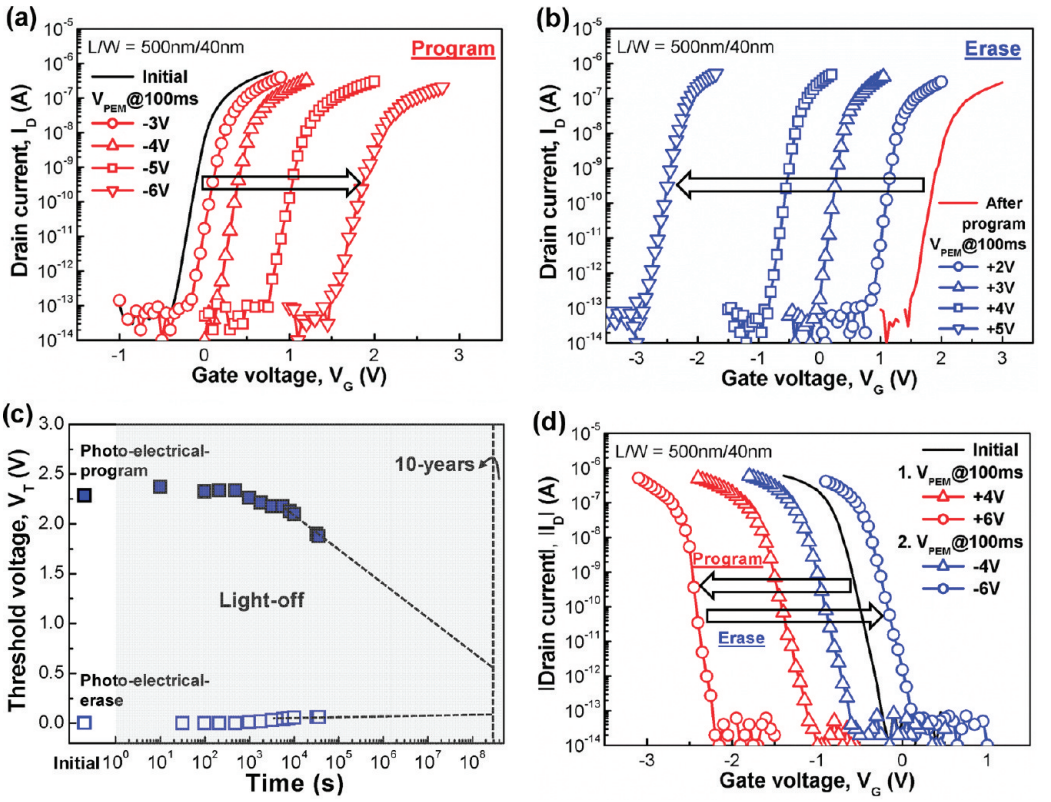

Figure 4. The photoactive characteristics of a Si-NW FET. (a) Positive V_T shift in n-type Si-NW FET with a combination of negative gate voltage and white light (for program). (b) Negative V_T shift in n-type Si-NW FET with a combination of positive gate voltage and white light (for erase). (c) Charge-retain ability through observation of the V_T decay with time. (d) The photoactive characteristics of the p-type Si-NW FET. The V_T shift trend of the p-type Si-NW FET by changing the gate bias polarity is the same as that of the n-type Si-NW FET.

positive shift of the I_D-V_G curve according to the negative gate voltage with duration (t_{PEM}) of 100 ms combined with white light of 100 mW cm^{-2}; this set of conditions is referred to as a photoelectrical program (Figure 4a). As the applied negative gate voltage (V_{PEM}) with fixed intensity of white light increases, the amount of positive shift increases. It is remarkable that the V_{PEM} value of the photoactive Si-NW FET is considerably smaller than that of a typical Flash memory.[17] Moreover, in terms of utilizing light absorption as a source for memory operation, the vertically standing nanogaps have a structural advantage of being directly open to absorb incident photons efficiently without any loss.

The V_T change by parallel shift of the I_D-V_G curve indicates that the combination of negative electrical pulse and optical pulse generates a certain amount of charges in PCBM. Furthermore, the positive direction of the V_T shift confirms that effective charges by the combined pulses have negative polarity.[18]

Meanwhile, positive gate voltage combined with white light causes a negative shift of the I_D-V_G curve from the photoelectrical-programmed state (Figure 4b). Opposite to the photoelectrical program, the additional charges generated by a combination of positive electrical pulse and optical pulse have opposite polarity, namely, positive polarity. These phenomena are thus collectively referred to as photoelectrical erase. As the positive V_{PEM} with fixed intensity of white light increases, the amount of the negative shift increases, and the resultant V_T finally surpasses the initial V_T value. Figure S4 in the Supporting Information summarizes the V_T change by photoelectrical program and erase according to the duration of program and erase bias with 100 mW cm^{-2} of white light, respectively.

Figure 4c shows the retain ability, that is, the retention time for the stored data in the photoactive n-type Si-NW FET. The Si-NW FET device is retained with the light off after a photoelectrical program of −6 V and photoelectrical erase of +5 V, and then the V_T decay, which is a criterion of the capability in charge storage, is measured with time. A small V_T decay after 10^4 s is observed. Extrapolation conveys that the retention time can meet the requirement of 10-years lifetime, which is the *de facto* industrial standard of retention time for Flash memory. Both retention time and repeatability characteristic also reveal that the proposed device can be used for nonvolatile memory applications (Figure S5 in the Supporting Information).

Moreover, the PCBM-embedded p-type Si-NW FET shows photoactive characteristics as well. Notably, the same V_T behaviors as those displayed by the n-type

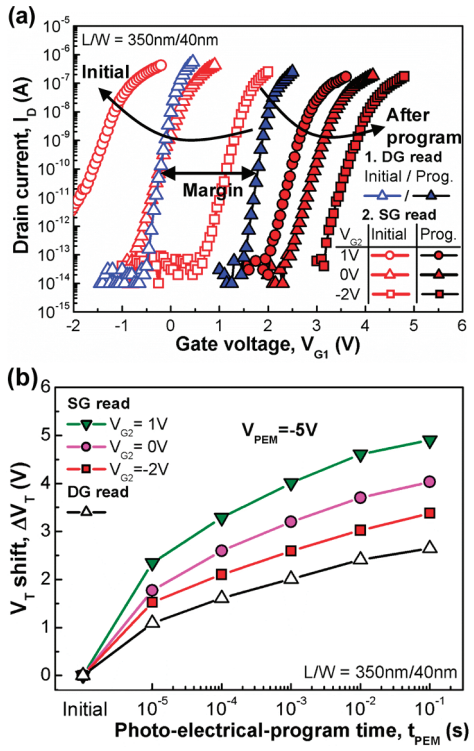

Figure 5. (a) I_D–V_G curves according to Gate 2 bias, read by sequential SG and DG modes after the DG program (V_{PEM} = −5 V, t_{PEM} = 1 ms). The V_T difference between the initial and programmed states represents the read margin. (b) The summarized V_T read margin according to t_{PEM}, through the SG read and DG modes after the DG program.

Si-NW FET are observed according to the polarity of the gate bias, as shown in Figure 3d. In other words, the phenomena in the p-type Si-NW FET ensure a photoactive characteristic, including the aforementioned charge distribution in the n-type Si-NW FET by photoelectrical program and erase. Hereafter, experiments are thus conducted with the n-type photoactive Si-NW FET.

In recent Flash memory technology, reduction of program voltage is an impending issue from the viewpoints of device reliability and chip density.[19,20] Figure 5a compares program efficiency in photoactive Si-NW FETs after DG-program according to the gate bias mode as a data-reading method. The V_T at each read mode is sequentially measured in the same device after −5 V DG-program with 1 ms-t_{PEM} under white light. The V_T difference between the initial and photoelectrical-programmed state is defined as the read margin. While the device read with the DG mode exhibits a margin of 2 V, the device read with the SG mode exhibits a wider margin than that with the DG mode even though the same amount of charges is distributed. In addition, as more positive Gate 2 bias is applied, a wider margin can be achieved. Figure 5b shows the V_T changes of the photoactive Si-NW FET with the DG and SG modes according to the t_{PEM}. These improved characteristics originate from optical gating[21] of the generated charges, which are located close to the supporting gate, as indicated in the Supporting Information (Figure 6).

CONCLUSIONS

In summary, memory function based on photoactive characteristics in n-type and p-type Si-NW FETs was demonstrated by the integration of solution-processable PCBM in a CMOS-compatible nanogap structure. By virtue of a separated gate structure and optical source, improved memory performance with lowered program voltage was achieved. This kind of hybrid integration with electrical and optical methods paves the way toward a new area of optoelectronic research based on maximizing the capability of 1-dimensional NW and compatibility to CMOS-processes in relation to platform technology.

METHODS

The fabrication process for a photoactive n-type Si-NW FET is similar to that of the "independent double-gate nanowire" process except for the additional nanogap formation for PCBM insertion. First, a 10^{15} cm^{-3} p-type silicon-on-insulator (SOI) wafer, with top silicon of 100 nm and buried oxide (BOX) of 140 nm, is prepared (Figure S1a in Supporting Information). After deposition of a 50 nm thick silicon–nitride as a hard mask, the NW is patterned with silicon–nitride (Figure S1b). Then, a 30 nm thick tetraethylorthosilicate (TEOS) sacrificial layer and 300 nm thick polysilicon gate electrode are sequentially deposited. The tied gate is separated by chemical mechanical polishing (CMP) with silicon–nitride as an etch-stopper (Figure S1c), and the gate electrode is patterned. After the source/drain is doped with As ion implantation, nanogaps between the gate electrode and the NW are created by a wet-etchant (Figure S1d). To make gate dielectrics, the device is reoxidized at 700 °C for 30 min. After gas annealing is formed under hydrogen ambient, the device is immersed in PCBM solution and subsequently dissolved in chlorobenzene with 5 mg mL^{-1}, for 24 h (Figure S1e). After it was spin-coated to remove unwanted PCBM residue, the device is dried at 150 °C for solvent evaporation. In the case of the p-type Si-NW, the overall process is the same as that for the n-type Si-NW, except for the dopant type and concentration of top silicon in the SOI wafer and source/drain.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Detailed fabrication process of photoactive Si-NW FETs, white-light effect of photoactive Si-NW FET, and simulation results according to the position of charges generated by the photoelectrical program are analyzed. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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